IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Daniel C. EDELSTEIN et al.	Group Art Unit: 2813
Serial No.	:	10/707,996	Confirmation No. 1995
Filed	:	January 30, 2004	Examiner: L. M. Schillinger
For	:	**DEVICE AND METHODOLOGY FOR REDUCING EFFECTIVE DIELECTRIC CONSTANT IN SEMICONDUCTOR DEVICES**	

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window, Mail Stop _____
Randolph Building
401 Dulany Street
Alexandria VA 22314

Sir :

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, Applicants respectfully bring the following documents, listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application.

Applicants note that this Supplemental Information Disclosure Statement is being filed after the issuance of an office action. Therefore, applicants hereby authorize the Commissioner to charge any fees necessary to ensure consideration of the documents cited herein to Deposit Account No. 09-0458.

Applicant respectfully requests that the Examiner consider the materials cited and indicate such consideration by appropriately initialing the enclosed PTO-1449 Form and including a copy of the initialed form in the next official communication.

Should there be any questions concerning this application, the Examiner is invited to contact the undersigned at the below listed telephone number.

Respectfully submitted,
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FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. FIS920030232US1	Application No. 10/707,996
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant Daniel C. EDELSTEIN et al.	
	Filing Date 01/30/2004	Group 2813

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

			V. Arnal, et al., "A Novel SiO_2 Air Gap Low K for Copper Dual Damascene Interconnect." Conference Proceedings of the Advanced Metallization Conference 2000, pp. 71-76
			A. P. Li, et al., "Hexagonal Pore Arrays with a 50-420 nm Interpore Distance Formed by Self-Organization in Anodic Alumina." Journal of Applied Physics, vol. 84, no. 11, December 1, 1998, pp. 6023-6026
			O. Jessensky, et al., "Self-Organization Formation of Hexagonal Pore Arrays in Anodic Alumina." Journal of Applied Physics, vol. 72, no. 10, March 9, 1998, pp. 1173-1175.
			A. P. Li, et al., "Polycrystalline Nanopre Arrays with Hexagonal Ordering on Aluminum." Journal of Vacuum Science and Technology, vol. 17, no. 4, July/August 1999, pp. 1428-1431.
			L.G. Gosset, et al., "General Review of Issues and Perspectives for Advanced Copper Interconnections Using Advanced Copper Interconnections Using Air Gaps as Ultra-Low K Material." IEEE 2003, pp. 65-67.
			V. Arnal, et al., "Integration of a 3 Level Cu - SiO_2 Air Gap Interconnect for Sub 0.1 micron CMOS Technologies." IEEE 2001, pp. 298-300.
			C.T. Black, et al., "Integration of Self-Assembled Diblock Copolymers for Semiconductor Capacitor Fabrication." Applied Physics Letters, vol. 79, no. 3, July 16, 2001, pp.409-411
			Z. Liu, et al., "Metal Nanocrystal Memories – Part I: Device Design and Fabrication." IEEE Transactions on Electron Devices, vol. 49, no. 9, September 2002, pp.1606-1613.

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.